

Challenges to Extending Semiconductor Cooling Limits

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The power problem associated with historic scaling of transistor technology has been well documented. While many efforts are underway to reduce leakage currents and employ more power-efficient architectures, the fact remains switching CMOS circuits consumes power. Therefore, even if these efforts succeed, the need for increasing levels of performance in all applications demands understanding where cooling limits exist and what options exist to extend them. Having a firm grip on these two aspects is required to define a viable strategy for delivering compelling products in a power-constrained world. This presentation focuses first on outlining where thermal limits exist today and what is causing the constraint. While it is impossible to define a specific power level that will make current cooling methods insufficient, these underlying issues provide the ability to identify where there will be a high risk of problems for specific applications. Secondly, it highlights what technology options exist to increase thermal capacity and the barriers each one faces to achieve adoption as a mainstream solution. This essentially lays the groundwork for extending the industry's ability to continue improving product capabilities through increased performance.